

80C187 Replacement Module Installation & Data Sheet

(Order.-Code: P.NPDA01)

Installation

WARNING NOTES

- The installation should only be performed by a qualified and technically experienced specialist. The device must be installed in compliance with the relevant DIN/VDE regulations or corresponding national standards.
- Trouble-free and safe operation of the unit is dependent on proper transport and storage, as well as installation by qualified personnel.

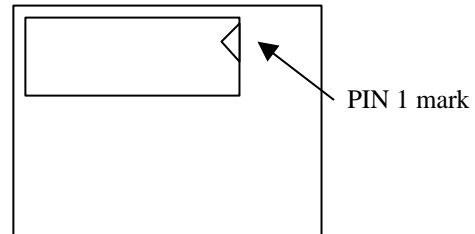
- Static Sensitive Device. Handle only at static safe work stations



- **Attention:** Wrong polarity, connecting the module under power on conditions, and electrostatic discharges can destroy the module.

INSTALLATION

- Remove power supply from basis board before connecting the 80C187 replacement module.
- Plug the 40-pin DIP connector of the 80C187 replacement module into the co-processor socket of the basis board
- Take care of correct orientation of connector and socket. Check PIN 1 mark!



*Seen from component mounting side
through the pcb.*

PRODUCT DESCRIPTION

The 80C187 replacement module is a fully compatible replacement of the Intel 80C187 processor.

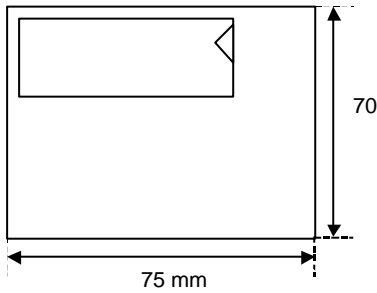
Technical Specifications

TECHNICAL DATA

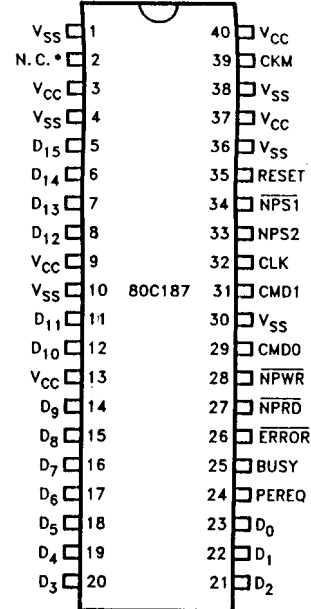
Supply voltage	5 V DC
Voltage on any pin with respect to ground	-0.5V to $V_{CC}+0.5V$
Power consumption	< 5 W
Temperature	Operating 0 - 55 °C * Storage -20 - +85 °C
Relative humidity	Class F (DIN 40 040)
Type of protection	IP 20
Dimension	75*11.8*70 [mm]
Connector	DIP 40

*) use of commercial components, use of automotive components possible at additional cost

DIMENSIONAL DRAWING



CONNECTOR PIN ASSIGNMENT



Device Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	Test Conditions
VCC	Supply voltage	4,75	5,25	V	
VIH	Input high voltage	2	$V_{CC}+0,3$	V	
VIL	Input low voltage	-0,3	0,8	V	
VOH	Output high voltage	2,4		V	IOH = -4mA
VOL	Output low voltage		0,45	V	IOL = 12mA
II	Leakage Current		+/-10	UA	
CI/O	I/O Pin Capacitance		10	PF	f = 1,0 MHz
tR/F	Input rise/fall time		40	Ns	
Tdwh (t6)	Data Setup to \overline{NPWR} (rising)	15		Ns	
Twhdx (t7)	Data Hold from \overline{NPWR} (rising)	10		Ns	
Trlrh (t8)	\overline{NPRD} Active Time	40		Ns	
Twlwh (t9)	\overline{NPWR} Active Time	40		Ns	
Tavwl (t10)	Command Valid to \overline{NPWR} (falling)	0		Ns	
Tavrl (t11)	Command Valid to \overline{NPRD} (falling)	0		Ns	

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Tmhr1 (t12)	Min Delay from PEREQ Active to /NPRD Active	20		Ns	
Twhax (t18)	Command Hold from /NPWR (rising)	8		ns	
Trhax (t19)	Command Hold from /NPRD (rising)	8		ns	
Tcmdi (t26)	Command Inactive Time	35		ns	
Txxcl (t20/21/24/25)	xx to CLK Setup	-	-	ns	CLK not used

Timing Responses

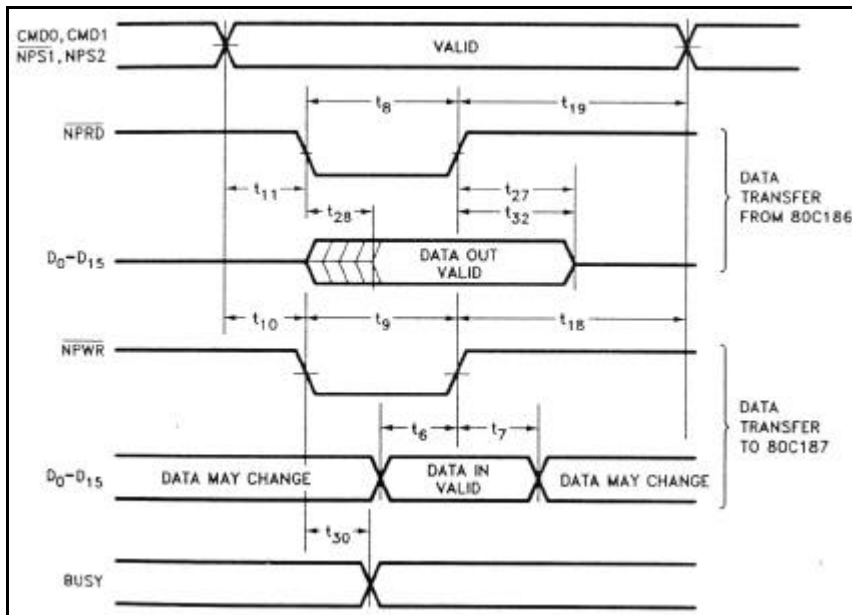
Symbol	Parameter	Min	Max	Units	Test Conditions
Trlqv (t28)	/NPRD Active to Data Valid		35	ns	
Trhqh (t32)	Data Hold from /NPRD Inactive	2		ns	
Trhqz (t27)	/NPRD Inactive to Data Float		15	ns	
Tilbh (t29)	/ERROR Active to Busy Inactive	250		ns	
Twlbv (t30)	/NPWR Active to Busy Active		60	ns	
Tklml (t31)	/NPRD or /NPWR Active to PEREQ Inactive		60	ns	
Trlhb (t33)	Reset Inactive to BUSY Inactive		60	ns	

Clock Timings

Symbol	Parameter	Min	Max	Units	Test Conditions
Tch/clxx (t1/2/3/4/5)	Clock	-	-	ns	CLK not used

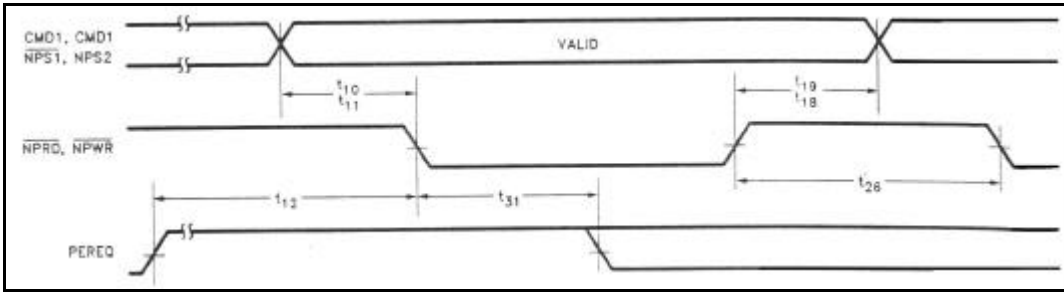
TIMING DIAGRAMS

Data Transfer Timing (initiated by CPU)

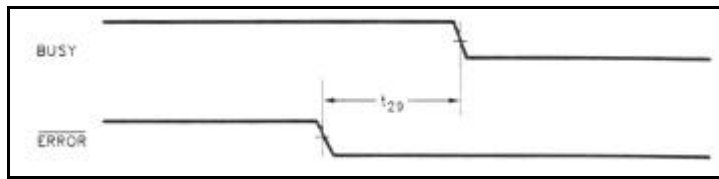


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Data Channel Timing (initiated by 80C187)



Error Output Timing



CLK, Reset Timing (CKM = 1)

